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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/584,778	XIONG, GUOPING	
	Examiner	Art Unit	
	RALPH A. VERDERAMO III	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1,3,6 and 7* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,3,6 and 7* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 3 recites the limitation "the other flash chip" in line 2. There is insufficient antecedent basis for this limitation in the claim. Previous instances of "the other flash chip" in claim 1 were amended to "said another one flash chip".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Estakhri et al. US Patent No. 6081878 (herein after referred to as Estakhri) in view of Klein et al. US Patent No. 5671439 (herein after referred to as Klein).

Regarding claim 1, Estakhri describes a data write-in method for a flash memory, wherein the flash memory comprises at least two flash chips **(flash memory chips 670 and 672 of Fig. 6 (column 6, lines 23 – 52))** and a controller **(controller 510 of Fig. 6 (column 6, lines 23 – 52))**. While Estakhri does describe one particular interleaving method **(Fig. 13)**, Estakhri does not specifically describe the method comprising: partitioning physical blocks in the at least two flash chips such that the physical blocks in one of the at least two flash chips have odd logical block addresses and the physical blocks in another one of the at least two flash chips have even logical block addresses; the controller receiving a data write-in instruction and analyzing a beginning logical address for writing from the received data write-in instruction; the controller obtaining the logical block address needed to be written according to the analyzed beginning logical address; the controller determining a parity of the obtained logical block address, and selecting one flash chip from the flash chips according to the determined parity of the logical block address; the controller directing a first programming or erasing instruction to the physical blocks corresponding to the obtained logical block address in the selected flash chip; the controller detecting whether said another one flash chip needs to be programmed or erased while the first programming or erasing instruction are being processed; if programming or

erasing is needed in said another one flash chip, the method further comprises: the controller directing a second programming or erasing instruction to said another one flash chip of at least two flash chips.

Klein describes a data write-in method for a flash memory **(It will be appreciated that other physical mass storage devices may be used...Examples include...flash memories...(column 14, line 66- column 15, line 5))**, wherein the flash memory comprises at least two flash chips **(Drive A and Drive B of FIG. 2)**, and the method comprises: partitioning physical blocks in the at least two flash chips such that the physical blocks in one of the at least two flash chips have odd logical block addresses and the physical blocks in another one of the at least two flash chips have even logical block addresses **(means for alternately transferring even-numbered blocks of physical sectors between the on-board memory of the first drive and the main processing system and transferring odd-numbered blocks of physical sectors between the on-board memory of the second drive and the main processing system (column 4, lines 36 - 41))**; receiving data write-in instruction and analyzing a beginning logical address for writing from the received data write-in instruction **(The preferred routine preferably receives as input a starting logical sector START (column 8, lines 16 - 18). Retrieve xfer command 102 of FIG. 2. Furthermore over the course of time that this invention is operating it will retrieve a plurality of xfer commands)**; obtaining the logical block address needed to be written according to the analyzed

beginning logical address; determining a parity of the obtained logical block address, and selecting one flash chip from the flash chips according to the determined parity of the logical block address **(Starting sector on drive A? 132 of FIG. 2)**; directing first programming or erasing instructions to the physical blocks corresponding to the obtained logical block address in the selected flash chip **(Starting sector on Drive A 132 of FIG. 2 following either YES path to Drive A Ready? 136 or NO path to Drive B Ready? 146)**; detecting whether said another flash chip needs to be programmed or erased while the first programming or erasing instruction are being processed **(More? 142 of FIG. 2. For example first-in/first-out (FIFO) register and/or direct memory access (DMA) circuitry may be used to temporarily store information related to a non-selected physical device while a transfer is occurring between a selected physical device and the host computer memory. Then once the transfer is complete on the selected device the information from the non-selected device may be burst into or from the main memory at an extremely high rate by the FIFO and/or DMA circuitry (column 8, lines 1 - 10))**; if programming or erasing is needed in in said another one flash chip, the method further comprises: directing a second programming or erasing instruction to said another one flash chip of at least two flash chips **(More? 142 of FIG. 2 following YES path to Drive B Ready? 146)**. Klein essentially describes a specific mapping method that allows for faster data transfer by sending odd logical blocks to one memory and even logical blocks to a different memory. The mapping

method could obviously be applied to the flash memory configuration of Estakhri where the controller would direct access between the two flash chips.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the interleaving method described by Klein in the flash memory of Estakhri because Klein explains that using this method overall sustainable data transfer rates may be improved by requesting the physical devices to begin access at substantially the same time **(column 3, lines 14 – 18)**.

Regarding claim 3, Estakhri in view of Klein describe the data write-in method for a flash memory according to claim 1 **(see above)**. Estakhri does not specifically describe wherein if the other flash chip does not need to be programmed or erased, the method further comprises: judging whether the processing of the first programming or erasing instruction is finished.

Klein describes wherein if the other flash chip does not need to be programmed or erased, the method further comprises: judging whether the processing of the first programming or erasing instruction is finished **(No path from More? 142 of Fig. 2)**.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the interleaving method described by Klein in the flash memory of Estakhri because Klein explains that using this method overall sustainable data transfer rates may be improved by requesting the physical

devices to begin access at substantially the same time **(column 3, lines 14 – 18)**.

Regarding claim 6, Estakhri in view of Klein describe the data write-in method for a flash memory according to claim 1 **(see above)**. Estakhri does not specifically describe wherein the analyzing further comprises: obtaining the number of sectors needed to be written from the data write-in operation instruction.

Klein describes wherein the analyzing further comprises obtaining the number of sectors needed to be written from the data write-in operation instruction **(Calculate starting and total sectors for drives A & B 200 of Fig. 2)**.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the interleaving method described by Klein in the flash memory of Estakhri because Klein explains that using this method overall sustainable data transfer rates may be improved by requesting the physical devices to begin access at substantially the same time **(column 3, lines 14 – 18)**.

Regarding claim 7, Estakhri in view of Klein describe the data write-in method for a flash memory according to claim 6 **(see above)**. Estakhri does not specifically describe that the analyzing further comprises: judging whether the data write-in instruction has been finished by subtracting a number of written sectors from a number of sectors needed to be written.

Klein describes that the analyzing further comprises: judging whether the data write-in instruction has been finished by subtracting a number of written sectors from a number of sectors needed to be written **(338 and 340 of Fig. 5(b))**.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the interleaving method described by Klein in the flash memory of Estakhri because Klein explains that using this method overall sustainable data transfer rates may be improved by requesting the physical devices to begin access at substantially the same time **(column 3, lines 14 – 18)**.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 3, 6 and 7 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RALPH A. VERDERAMO III whose telephone number is (571)270-1174. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RALPH A VERDERAMO III/
Examiner, Art Unit 2186

rv
October 18, 2011

/Pierre-Michel Bataille/
Primary Examiner, Art Unit 2186